Voltage Dependence of Ferroelectric Class 2 Multilayer Ceramic Capacitors

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ABSTRACT

We review the physical background of the voltage-dependent capacitance of class 2 Multilayer Ceramic Capacitors (MLCC) and present models for this dependency. Two processes can be distinguished, leading to an immediate as well as a long-term capacitance dependence on DC voltage. Both processes are related to the ferroelectric properties of class 2 materials. The immediate process is related to the dipole reorientation within the material domain structure. The origin of the long-time DC effect, still discussed in the scientific community, is likely to be related to domain wall movement. We will also discuss the influence of the two processes on the application of MLCCs.

I. MOTIVATION AND BACKGROUND

For the design-in process, it has become a common procedure to employ simulation software such as SPICE. The developer may load files for multilayer ceramic capacitors (MLCCs) into the software to simulate the influence of the voltage and frequency behavior of the MLCC on the circuit. To make this simulation computationally efficient, it is necessary to implement elegant mathematical models for the MLCCs.

This article briefly reviews the physical background of the voltage-dependent capacitance of class 2 MLCCs. Furthermore, it describes the mathematical polarization model's development, suitable for simulation software implementation. An important dielectric property that ceramics can exhibit is ferroelectricity. Ferroelectricity describes the property of a material to form electric dipoles without applying an electric field. Ferroelectricity only occurs in crystals that have a unit cell with no center of symmetry, i.e. non-centrosymmetric shape.[1,2,3,4,5]

In a ferroelectric material, such as barium titanate, all direct and indirect neighboring cells form the aforementioned dipoles, which point in the same direction. Figure 1 depicts a simplified unit cell of the barium titanate unit cell with a permanent dipole. The alignment of neighboring dipoles is a result of total energy reduction due to dipole-dipole interactions. The ferroelectric attempts to attain a domain configuration that minimizes the total energy while satisfying both electrostatic and mechanical boundary conditions. [6] In an idealized system, all the dipoles in the crystalline material would collectively point in one direction. Real materials, however, always have minor imperfections that cause the collective orientation of the dipoles to be limited to areas called domains. The size of the domains, crystal configurations at domain boundaries and the orientation of the dipoles within the domains influence the polarizability and, thus, the permittivity of the material.[7,8] This is why MLCCs produced from different raw materials will have different ferroelectric behavior.[1,9,10]

Above the Curie temperature, which is specific for each ferroelectric material, this collective alignment is destroyed. In this phase, the dipoles are randomly aligned and no longer show a domain structure. Under these conditions, the material has paraelectric properties.[11] Ferroelectric materials always show some degree of paraelectric behavior. Paraelectricity may also be induced by chemical additives, which introduce defective sites and consequently prevent the formation of domains.

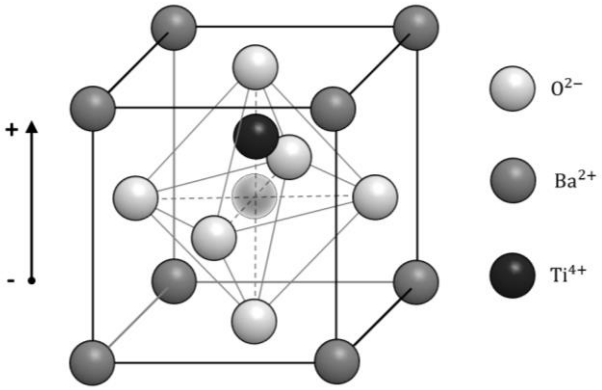

Figure 1 Configuration of the barium titanate unit cell below the Curie temperature. The barium ion is shifted from the center of the unit cell along the vertical axis. The shift is permanent and caused by internal stress of the unit cell.

Compared to other materials, ferroelectrics, such as barium titanate, have a high polarizability and thus, a high relative permittivity. Barium titanate-based MLCCs have the benefit of combining low losses with high capacitance and small structural shape. This property makes MLCCs one of the most important passive components for switching converter circuits and filter applications.[10]

The trade-off for the large capacitance in ferroelectric class 2 MLCCs is the above-mentioned voltage dependence that leads to a disadvantageous decrease of capacitance with increasing DC voltage. In the further course of this article, we will first explain the polarization processes and second develop a model, designed to describe the voltage-dependent capacitance.

II. EXPERIMENTAL DETAILS

Before the measurements, all capacitors (885012209073) have been annealed for at least 1 h at 150°C. The subsequent cool-down time was 24 h. All measurements were performed at room temperature.

For the hysteresis and time-dependent measurement, the LCR meter E4980A from Keysight was used in conjunction with the test fixture 16034G. The ac probing voltage amplitude of the LCR meter was $V_{rms} = 1\,V$ and the corresponding probing frequency was 1 kHz. The Automatic Level Control guarantees the fixed signal amplitude, which monitors the voltage level at the DUT and adapts the voltage level at the source.

III. IMMEDIATE POLARIZATION EFFECTS ON CAPACITANCE-VOLTAGE MEASUREMENTS

Ferroelectric polarization is well studied and shall be reviewed briefly.[1,9,13] The polarization behavior of ferroelectric materials depends on the actual state of polarization, as shall be discussed with the capacitance-voltage and polarization-voltage graphs of a 10 µF MLCC (X7R class 2), shown in Figure 2. The choice fell on this capacitor since it shows a pronounced dc-dependence, which is typical for this type.

During the measurement, a sinus probing waveform of frequency f is applied to measure the capacitance of the capacitor. The ac probing waveform has a fixed amplitude throughout the measurement and induces a periodical change of voltage $\mathrm{d}V$. On the sinus signal, a dc voltage is superimposed, allowing the reorientation of the domain polarization. This reorientation takes place on a sub-second time scale and is thus an immediate polarization effect.

Branch 1 (dashed green):

The capacitor, with randomly distributed domain polarizations, is subjected to the test signal. With the increase of dc voltage, the dipoles eventually become aligned, leading to increased polarization (Figure 2). The saturation polarization is reached, if all dipoles point in the direction of the external electric field (dc-voltage). As the voltage increases, the dipoles become aligned and the dipole movement becomes more restricted, which leads to a reduced change of charge $\mathrm{d}q$. Hence, the capacitance $C = \frac{dq}{dV}$ decreases with increasing dc voltage.

When the applied external field E, which is proportional to the applied voltage, has aligned the majority of the domains, the dipoles remain in this position even without the external field. The collective alignment creates an internal stabilizing coercive field, E_c. As the applied electric field increases, the overall polarization increases due to electronic, ionic and dipolar polarization effects.

The polarization at maximum voltage is referred to as saturation polarization P_{sat}. In principle, the spontaneous polarization P_s is equal to the saturation polarization of the electric displacement extrapolated to zero field strength.

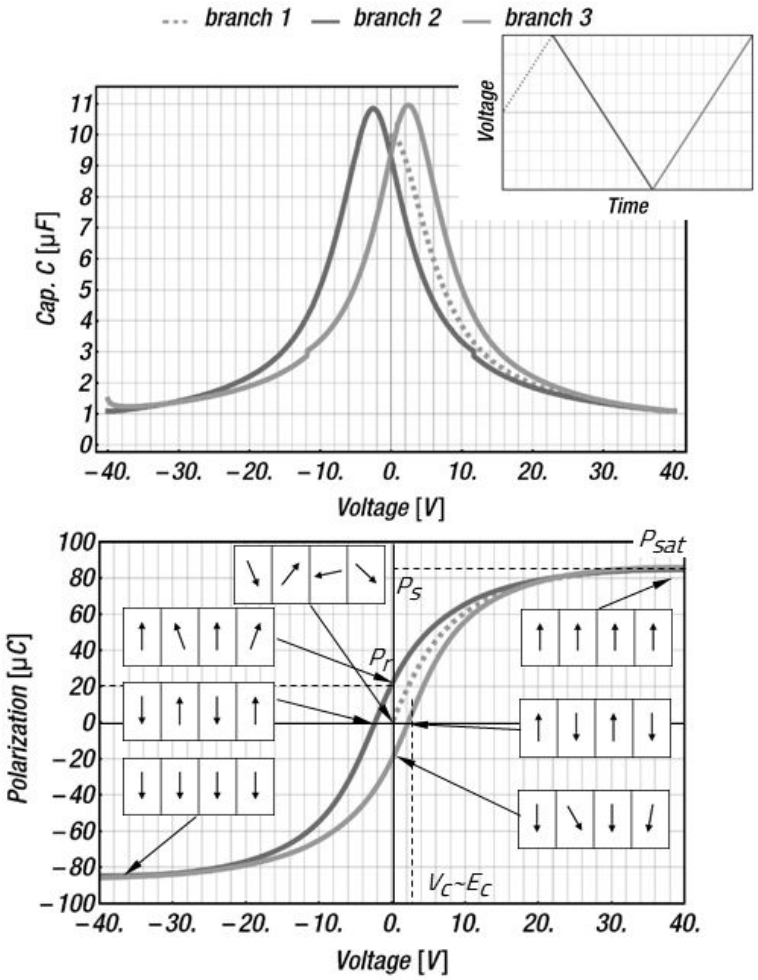

Figure 2 TOP: Measured capacitance-voltage characteristics of 10µF MLCC, for a dc voltage cycle, shown in the inset graph. BOTTOM: Polarization-voltage characteristics with corresponding schematic depiction of dipole orientation.

Branch 2 (blue):

As the voltage, and thus, the external field, is reversed from positive to negative, the dipoles relax slightly but remain in their overall polarization direction due to the internal coercive field, E_c. The polarization state at zero volts is referred to as remanent polarization P_r.

Any reversed external electric field will have to exceed E_c in order to reorient all domains in the opposite direction. At the position of E_c the strain on the dipoles is least. Thus the permittivity of the material (susceptibility) is largest and the capacitance shows a local maximum. With the increase of polarization into the opposite direction, the capacitance decreases to the same value as for positive voltages.

Branch 3 (green):

If the voltage is driven from negative to positive, the dipoles reorient again when the externally applied field exceeds the coercive field. This, again, leads to a peak at the capacitance at positive voltages. The process is similar to the one described before. Branch 3 is similar to branch 2, except it is shifted along the x-axis toward positive voltages.

The above-described hysteresis requires the distinction between the polarizations for voltage sweeps from positive to negative and vice versa. Therefore, in the further course, $P^+(E)$ denotes the polarization (branch 2) for voltage sweeps from positive to negative and $P^-(E)$ (branch 3) the polarization for voltage weeps from negative to positive voltages.

Hence, any increase in dc voltage leads to a decrease in capacitance. However, the capacitance is further decreased with an increasing application time of dc voltage. That further decrease is related to the retarded movement of the domain walls, caused by domain wall pinning. [14,15,16,17,18] Domain wall motion takes place on a longer timescale than the initial reorientation of dipoles, which occurs on a sub-second timescale. [19] Domain wall movement generally leads to an additional gradual decrease of the capacitance of up to 20 %, which can take place over 1000 hours. [14,15]

Besides the domain wall movement, a field-induced phase transition may occur on some pristine barium titanate compounds [20,21]. During this process, the unit cell undergoes a structural change, forming the permanent dipole. This kind of phase transition causes a peak in the capacitance-voltage measurements even during the first sweep (Branch 1), which is similar to the one exhibited during the reorientation of the dipoles (in branch 2 and branch 3). Hence, the origin of the peak is not the reorientation of the dipoles but the reconfiguration of the unit cell in at least some fractions of the material. Such a behavior is not visible in this measurement shown here but may be in others.

The physics of ferroelectric and paraelectric materials are well discussed in scientific literature, which provides a solid basis for the development of a model suitable for technical applications such as electrical circuit simulation.[1,13,22,23] The parameters are related to measurable and physically meaningful quantities such as remanent and spontaneous polarization.

A model that is based on an ideal polarization behavior [13] is:

$$C(V) = (a - C_S)\, sech^{c}\left(\frac{V - V_C}{b}\right) + C_S \qquad (1)$$

with C_S as the quasi-linear contribution to the capacitance (voltage-independent pure capacitive part), V_C as the coercive voltage ($V_C \propto E_c$), a as the factor proportional to saturation polarization, b as the factor related to the width of the bell-shaped curve and c a slope form factor. The advantage of this model is that a, b, C_S and V_C can be retrieved directly from the measured data, i.e. no fitting is required. C_S is the capacitance at the maximum voltage, $(a - C_S)$ is the height of the peak (max. of $C(V)$), V_C is the position of the peak and b can be calculated from $C(V)$ with the inverse of the hyperbolic secant.

Whether or not the polarization model published initially by Miller et al. [13] is based on first principles is of no importance at this point. What is relevant is the numerical simplicity, since the parameters can be clearly related to characteristic features of the measured data. Consequently, this leads to a situation where the set of parameters is relatively small and easily retrievable from the measurement.

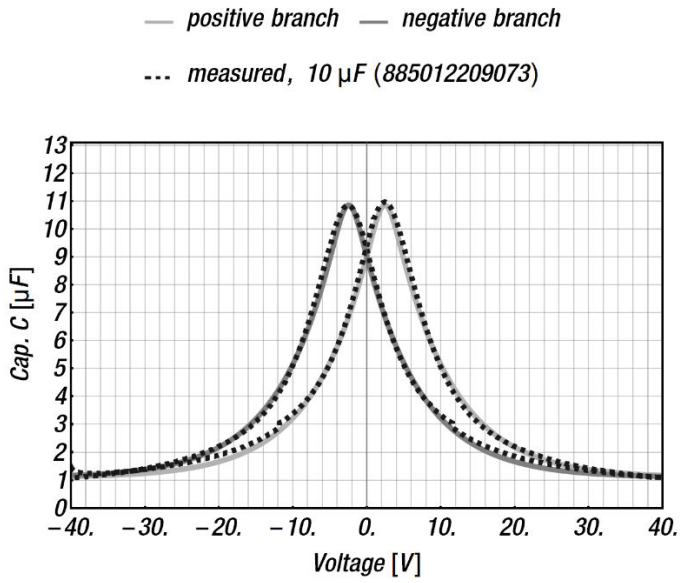

Figure 3 *Measured capacitance-voltage characteristic of 10 µF MLCC with the corresponding fit of equation 1. Dimensionless numerical fit-parameters: a =10.85, b = 1.3, c = 0.17, C_s = 1.09, V_C = 2.5.*

Figure 3 shows a C-V measurement of a 10µF class 2 MLCC, which was measured with consecutive voltage sweeps, along with a fitted equation (1). Although the fit is not perfect, especially the features between -10 V and+10 V are well described by the model. The two visible peaks of the positive and negative branch occur, if the external field reaches the coercive field strength and cause a reversal of the dipole orientation. At this moment, the dipoles have large mobility, i.e. the change of charge is large. Thus the capacitance has a local maximum at this position.[1]

IV. AGING EFFECTS ON CAPACITANCE-VOLTAGE MEASUREMENTS

A long-term effect, also known as aging or second-stage process, will lead to a further decrease of capacitance over time. For many years, there has been a discussion in the literature about the exact origin of this long-term capacitance decrease.[24, 25, 26, 27, 28]

To mention two of several possible explanations: Some propose that the reduction of dielectric permittivity is due to the permittivity difference between two domains with orientations of 90° to each other.[15] It is argued that with time the

domains with 90° polarization become orientated along the applied field. Since the domains with 90° polarization have higher polarizability than the ones parallel to the applied field, the overall permittivity is decreased as the 90° polarized domains are realigned.

Others propose that the effect is due to the diminished contribution of the domain wall region itself.[16] They argue that domain wall regions have comparatively large polarizability/permittivity and that the diminishing of the walls leads to a decrease in overall polarizability and, thus, the overall permittivity, i.e. capacitance decrease.

Both mentioned explanations are related to the retarded movement of the domain walls, caused by domain wall pinning. [14, 15, 16, 17]. This effect leads to a further gradual decrease of the capacitance upon applied dc voltages over a period of hours. Since domain wall movement is an essential process in several explanations, reviewing it in the following is worthwhile.

Figure 1 depicts a simplified unit cell that has a cubic structure. Due to structural stress within the lattice and/or applied electric fields, the unit cell can be stretched and tilted. This not only allows the displacement of the Ti-ion along this one vertical axis, as indicated in Figure 1, but also along other directions, leading to domains that have polarizations with an angle of 90° to each other, as is shown in Figure 4.[24] The boundaries between these domains, also known as 90° domain walls, are regions with higher polarizability than the domains themselves.[18]

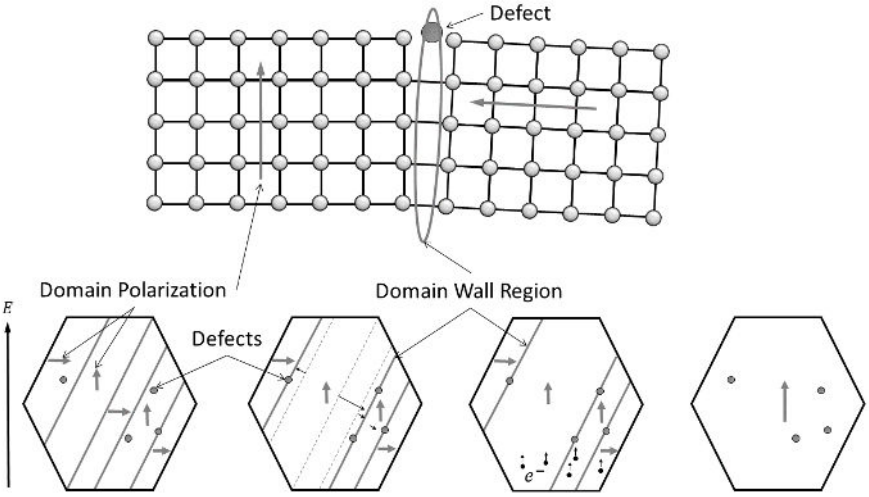

Figure 4 Schematic depiction of defect site in lattice (top) and simplified illustration of long-term process of domain wall motion under electric field application from its initial (bottom-left) to its final state (bottom-right).

Those domain walls stabilize their position at defect sites, i.e. defect dipoles. The continuous application of a dc field moves electrons to eliminate the defect dipoles with time. This enhances the domain-wall motion to align the 90° polarized domains of $BaTiO_3$ to the electric field direction.

We want to refrain from discussing further proposed explanations of the long-term process. Researchers have not yet agreed on a unified explanation of the aging process. No matter what process is causing the capacitance decrease, more critical for the practical application is the actual magnitude and description of the effect. The long-term effect is exemplified at a 10 µF MLCC (PN: 885012209073) with a rated voltage of 50 V, in Figure 5. The capacitance-time graphs are measured at 100%, 80% and 50% of the capacitor's rated voltage over a period of about 160 h. The measurement starts about 10 seconds after the application of the dc voltage. The graphs clearly show that the larger the dc voltage the larger the overall decrease of the capacitance. In this example, the saturation capacitance is reached in about 1 h or so. Other examples reach saturation after 10 h.[14,15] Beyond this time the capacitance remains almost constant or decreases at an even slower rate.

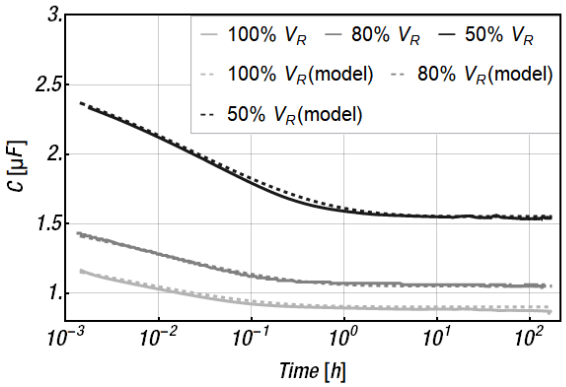

Figure 5 Measured capacitance vs. time for three different DC voltages. (Measurement frequency f=1 kHz) Measurement starts 10 seconds after the application of the DC voltage. The decrease of capacitance is associated to long-term polarization process.

It is worthwhile to point out that the decrease relative to the rated voltage, due to the long-term process, is less pronounced than for the immediate process. The relative capacitance in Figure 6 shows that the capacitance values start already between 23% (50% of V_R) and 12% (100% of V_R). The long-term decrease in this example is about 3%, 4% and 8% for 100% of V_R, 80% of V_R and 50% of V_R, respectively. This change is below the production tolerance of $\pm 10\%$. The lower the dc voltage the larger the additional capacitance decrease.

Even at very small or no dc voltage, the MLCC will experience a slight capacitance decrease of about 10% to 20% (relative to rated capacitance) over a time of about 1000 h.[15,28,29] This is typical behavior for this capacitor technology, although slight variations between different products may occur, depending on the grain size or the chemical additives of the used ceramic material.[15,16,19] The capacitance decrease is voltage as well as temperature dependent. Consequently, from an experimental point of view, measuring all parameters over such a long period of time is laborious. However, a prudent and practical rule of thumb is to add another 10% capacitance decrease for voltages above 50% of V_R and 20% capacitance decrease for dc voltages below 50% of V_R.

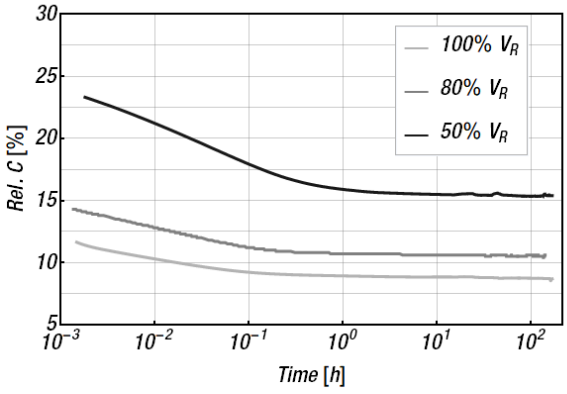

Figure 6 Measured relative capacitance vs. time for three different DC voltages in reference to V_R. (Measurement frequency f=1 kHz) Compare to Figure 5.

Some documentation or publication presents the relative change not in reference to V_R but to the decreased capacitance value after the immediate process. This has the effect that the relative change due to the long-term process appears larger in numbers. Such representation may be justified in one case or another; however, it neglects the capacitance decrease due to the effects of the first immediate process. Therefore, such representations do not provide information about the overall capacitance decrease and may, therefore, not directly be used by the electrical engineer for the calculations of effective capacitances.

A model of the long-time effect on the capacitance, related to physically measurable parameters, is

$$C_l(t) = (C_0 - C_\infty)Exp\left[-\left(\frac{t}{\tau}\right)^{\alpha}\right] + C_\infty \qquad (2)$$

with $C_0 = C(V)$ as capacitance at the beginning of the long-time process, C_∞ as saturation capacitance (at the end of the long-time process), τ as a characteristic time as well as α as form factor.[14, 26] The practicality of the model is exemplarily demonstrated in the measurements in Figure 5 with the parameters listed in Table 1.

Table 1 *Parameters as used for fitting the capacitance measurements in Figure 5.*

	$\boldsymbol{\alpha}$	$\boldsymbol{\tau}$	$\boldsymbol{C_0}$	$\boldsymbol{C_\infty}$
$\mathbf{50\%}\,\boldsymbol{V_R}$	0.3	0.025	2.8	1.55
$\mathbf{80\%}\,\boldsymbol{V_R}$	0.3	0.010	1.68	1.05
$\mathbf{100\%}\,\boldsymbol{V_R}$	0.3	0.005	1.4	0.9

V. CONCLUSION AND CONSEQUENCE FOR THE DESIGN-IN PROCESS

After introducing ferroelectricity, we have discussed the influence of immediate and long-term application of dc-bias voltage on capacitance measurements. The capacitance decrease due to the initial application is larger than for the subsequent long-term application. Although at lower voltages, the effect over the long-term becomes increasingly prominent. Thus, both effects have to be considered in the design-in process. It has been demonstrated mathematical models can well describe the effects. Since both models are related to physically meaningful parameters, they are well suited to be used in the design-in process to calculate the actual usable capacitance.

Consequently, for the circuit design, it is necessary to know the application-specific dc voltage load and operation time to make the right choice of MLCC. The best strategy is to anticipate the capacitance decrease and oversize in terms of rated voltage or capacitance accordingly. To do that, it is necessary to know the actual magnitude of the short as well as long-term capacitance decrease. For that, one may use educated approximations based on literature, actual measurements or models as implemented in the Würth Elektronik LTspice libraries. The mentioned LTspice models are based on actual measurements and specifically model the prominent short-term effect for each part.

To account for the long-time effect, it is most practical to add a further 10% capacitance decrease for voltages above 50% of V_R and 20% capacitance decrease for dc voltages below 50% of V_R. The fact that this long-time process is also taking place at zero voltages is relevant for applications with long off-times. It would, however, not have any adverse effect on parts with long storage times in warehouses before the actual assembly and soldering, since the soldering temperatures are above the Curie temperature.

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